

Design of ALU using reversible logic based Low Power Vedic Multiplier

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Abstract— Arithmetic Logic Unit (ALU) is a heart of microprocessor and microcontroller units that are playing main role in digital computers. By optimizing the ALU circuit in microprocessor and microcontroller highly power efficient digital system can be achieved. The use of low power and high performance sub-blocks like adder and multiplier can reduce the total power dissipation of ALU. So in this paper we are introducing new architecture for a high speed and area efficient Vedic multiplier and an adder circuit using reversible logic gates. The proposed adder and multipliers are employed in the implementation of Arithmetic Logic Unit (ALU) to reduce the power dissipation and area and to improve the performance sufficiently. Integration of low power sub-blocks of ALU resulted that the power dissipation of proposed ALU unit is reduced when compared with the conventional unit. The proposed logic blocks are implemented using Verilog HDL programming language, simulated and synthesized using Xilinx ISE 9.2i software.

Index Terms— ALU, Reversible Logic Gates, Vedic Multiplier, Divide and Conquer approach, HDL.

1 INTRODUCTION

The improvement of logic circuit integration in digital logic design is a great and wide development in computing machines. However the exponential growth of transistor density in an integrated circuit increases the power dissipation and area of the circuit tremendously. The reversible logic circuit marks a promising new direction for low power circuits. The reversible logic gate is an energy efficient logic that can be employed in arithmetic and logic circuits. The reversible logic circuits consume less power dissipation and provide distinct output assignment for each distinct input. The basic set of gates like NAND, AND, NOR, OR, XOR and XNOR are not reversible. So the reversible logic gates can be used to implement even the complex circuits with very less power dissipation and it is verified in [1]. Reversible logic gates has attracted the attention of many researchers in recent years for its enormous possibility of application in low power CMOS design,

quantum computing and nanotechnology. Reversible logic is used for low power computation and high speed computation and that verified in [2]. Also the reversible logic gates are widely compatible with revolutionary computing paradigms such as optical and quantum computing. The efficient adder circuits which have hardware complexity is required of carry skip adder architectures.

The logic implementation of complex adders were obtained in [3] for different logic techniques including reversible logic based adders. The implementation result verified that the implementation of complex adder is consuming less power and area with high performance. The logic adder circuit with reversible logic circuit is described in [4]. The paper [5] describes the implementation of an 8-bit Vedic multiplier enhanced in terms of propagation delay when compared with conventional multiplier like array multiplier, Braun multiplier, modified booth multiplier and Wallace tree multiplier. Also it verified that the propagation delay of extracted output is very less compared to conventional methods.

High speed pipelined multiplier architecture is proposed in the paper [6] and the synthesized results shows that multiplier implemented using Vedic multiplication is efficient in terms of area and speed compared to its implementation using Array and Booth multiplier architectures. The logic implementation of Vedic multiplier using reversible logic circuit is described in [7] in which the synthesis result shown that the power dissipation is less than the conventional circuits. The design of two programmable reversible logic gate structures targeted at ALU implementation and their use in the realization of an efficient reversible ALU is demonstrated. ALU design is verified and its advantages over the only existing ALU design are quantitatively analyzed. In paper [8] proposes a new gate called Parity Conserving Multi-Functional (PCMF) Gate which is Fault tolerant by its very nature which can be used to design effectively the components of an ALU.

The proposed gate has high flexibility as compared to its counterparts in literature. The adder with ripple-carry logic was selected as the best design and it is implemented in the design

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of a 32-bit arithmetic logic unit is demonstrated in [9] and [10]. The power and performance metrics were compared with the conventional ALUs built with the fast adders designed with dynamic logic style in [11]. Significant power reduction with the sub-threshold operating voltage is achieved. Also the design is compared with the ALU design proposed for reversible quantum computers in the CMOS context to show the logic efficiency of the proposed design around 30 % in area.

In this paper we are proposing a new ALU circuit with a Vedic multiplier which reduces the system area and power consumption of the circuit and Reversible logic circuit which consumes very less power. The logic blocks of ALU is implemented using Vedic multiplier and Reversible logic gates. The implementation of ALU is described in detail below.

2 PROPOSED ALU

The block diagram of proposed ALU is shown in Fig.1 which consists of an arithmetic unit, logic unit and a multiplexer. Arithmetic unit is designed to perform the arithmetic operations like addition, subtraction, multiplication and division. Logic unit is designed to perform the logic operations using basic logic gates with reversible logic. Multiplexer is used to select any one of the circuit operation either arithmetic or logic operation and directs the output of respective unit to the output terminals of ALU. The circuit design and implementation of sub-blocks are described in detail below.

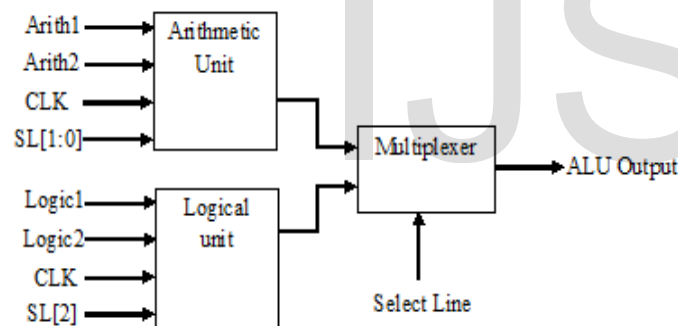


Fig. 1. Block Diagram of Proposed ALU

2.1 Arithmetic Unit

The logic blocks of arithmetic unit is designed using reversible logic gates and Vedic multiplier which are used to reduce the power dissipation and transistor count of arithmetic unit. The block diagram of arithmetic unit is shown in Fig.2. The reversible logic gate is employed to obtain the logic operation with low power dissipation.

2.1.1 Reversible logic gate

The logic block of a proposed reversible logic gate is shown in Fig.3 in which the reversible logic gate accepts three inputs and provides three outputs. One to one mapping technique is used in the reversible logic gate that helps to determine the outputs from input and that outputs can be used to recover the inputs. It satisfies the demand of Landauer's principle and C.H. Bennett rule that are defined for energy efficiency. The reversible gate can be used to perform all the logic gates with high speed and low area and power dissipation.

Reversible logic gate can be used to perform logical operations like AND, OR, NAND, NOR, Buffer, XOR, XNOR with high speed, less area and less complexity. In this logic at any instant of time one of the input acts as a control input and other two works as data input. The logic circuit computation using reversible logic gate improves the efficiency of the circuit with low power dissipation.

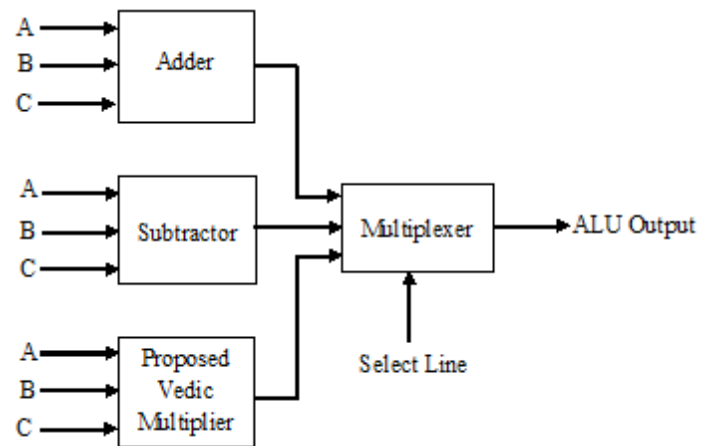


Fig. 2. Proposed Arithmetic Unit

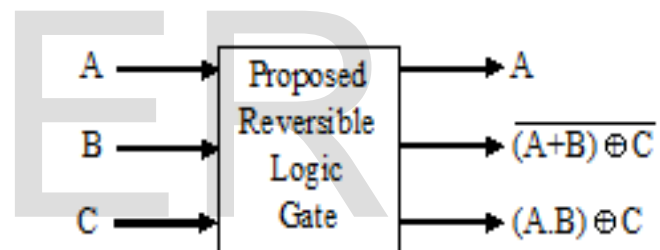


Fig. 3. Proposed Reversible Logic Gate

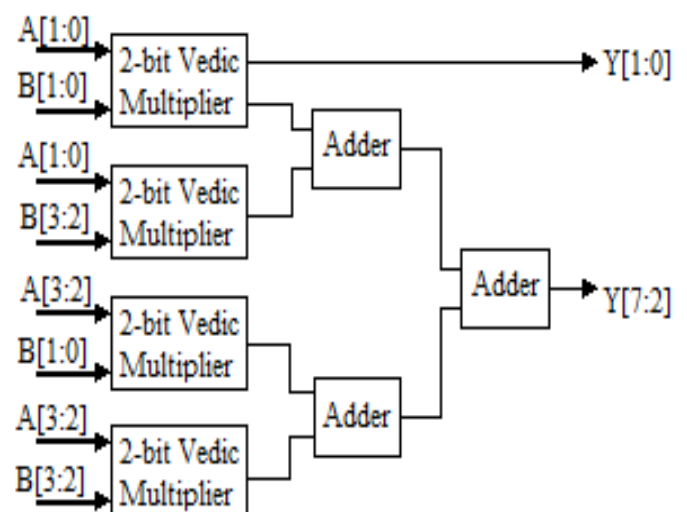


Fig. 4. Proposed 4-bit Vedic Multiplier

2.1.2 Vedic Multiplier

Usually multipliers are implemented in the digital system using multiple number of adders and such a multipliers are implemented with the help of array and booth's algorithms. But Vedic mathematics illustrates the multiplication operation very faster than other algorithms by reducing number of addition. The reduced number of adders in Vedic multiplier minimizes the operating delay and area of device with less number of adders. For example consider a $N \times N$ multiplier, it may require $N \times (N-2)$ full adders, N half-adders and $N \times N$ AND gates to perform the multiplication. But Vedic multiplier requires only $N-2$ gates and $(N-1)$ adders. Since the use of less number of adder Vedic multiplier occupy less area and consumes reduced power in logic implementation and operation respectively.

A proposed 4-bit Vedic multiplier is shown in Fig.4 in which the logic evaluation of multiplication process is performed using divide and conquer method. The logic multiplication of two 4-bit binary number with proposed Vedic multiplier is described below. Let us assume the binary inputs are A4A3A2A1 and B4B3B2B1. The output expressions of proposed Vedic multiplier are

$$\begin{aligned} X0[3:0] &= A[1:0] \times B[1:0] \\ X1[3:0] &= A[1:0] \times B[3:2] \\ X2[3:0] &= A[3:2] \times B[1:0] \\ X3[3:0] &= A[3:2] \times B[3:2] \end{aligned} \quad (1)$$

Then the logic addition of multiplied terms are performed as follows

$$\begin{aligned} Y[1:0] &= X0[1:0] \\ Y[2] &= X0[2] + X1[0] + X2[0] + 1'b0 \\ Y[3] &= X0[3] + X1[1] + X2[1] + 1'b0 \\ Y[4] &= X1[2] + X2[2] + X3[0] \\ Y[5] &= X1[3] + X2[3] + X3[1] \\ Y[7:6] &= X3[3:2] \end{aligned} \quad (2)$$

In this proposed logic the logic addition is performed using reversible logic gates which is an energy efficient arithmetic logic circuit in the digital system design.

The logic output of 4-bit Vedic multiplier is designed by the combinations of 2-bit Vedic multipliers. The block diagram of 2-bit Vedic multiplier is shown in Fig 5. It is implemented using the adders and logic gates.

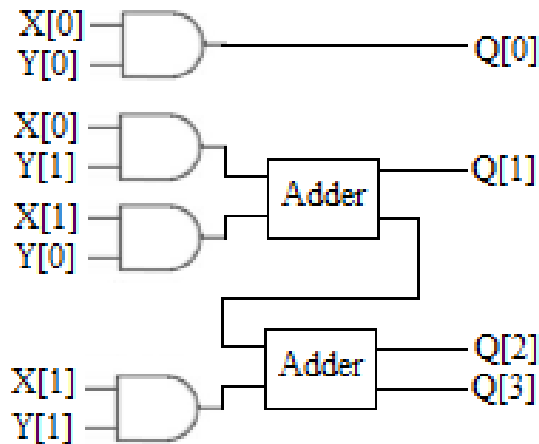


Fig. 5. Proposed 2-bit Vedic Multiplier

2.2 Logical Unit

The block diagram of logic unit is shown in Fig.6 which is consisting of a reversible logic gate and a multiplexer. The logic outputs of reversible gate are selected by the multiplexer. The energy efficient reversible logic gate is used to perform the logic operations with reduced power dissipation and area.

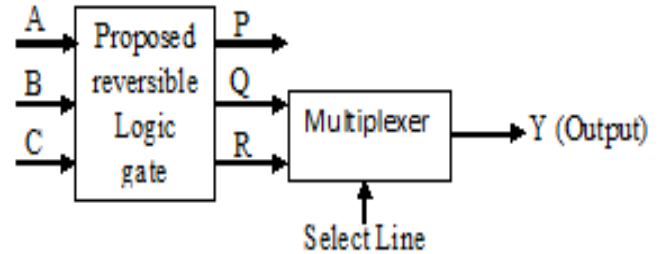


Fig. 6. Block diagram of Proposed Logical Unit

3 RESULT ANALYSIS

The proposed functional blocks of ALU circuit are implemented by using hardware description language. And the outputs are analyzed by comparing with the conventional architecture that results in the minimized power consumption and reduced area. All the presented high performance low power architecture outputs are implemented using Verilog Hardware Description Language (HDL) and synthesized in cadence RTL compiler using TSMC 0.18 μm CMOS technology library file. The low power techniques are synthesized to observe the power and area of each technique separately. Also by employing the low power techniques in ALU architectures, we obtained the power and area of proposed processors. The area and power of proposed structures are compared with conventional structure that results in the reduced power consumption and area, increased performance.



Fig. 7. Simulation result of Reversible Logic gate

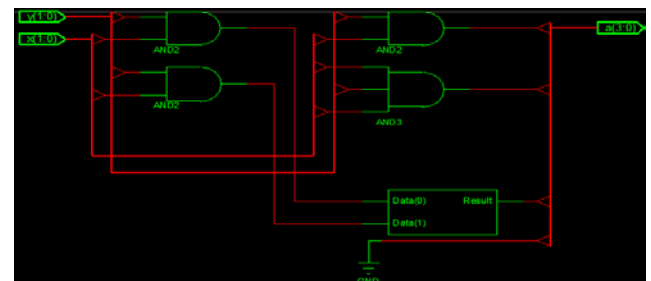


Fig. 8. Synthesized result of Reversible Logic gate

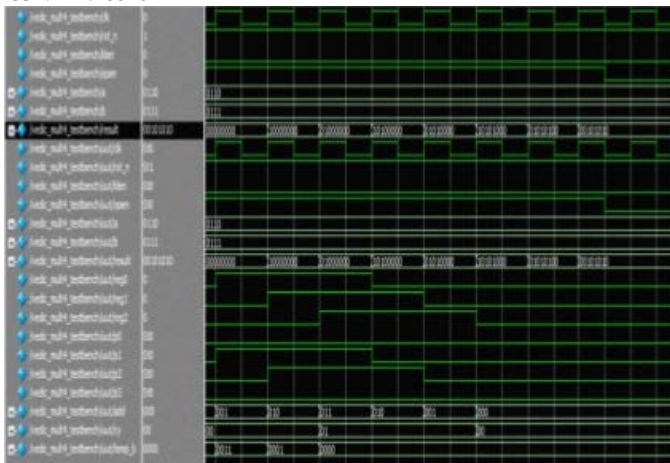


Fig. 9. Simulation result of 4-bit Vedic Multiplier

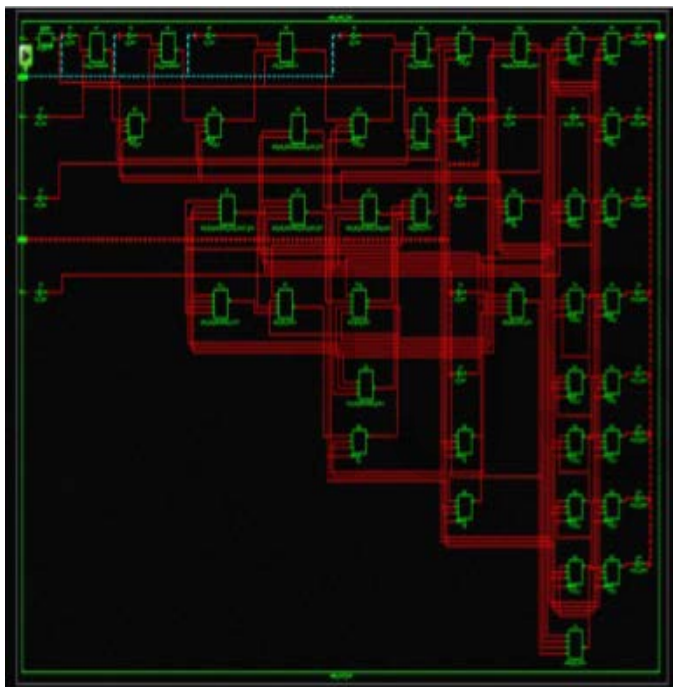


Fig. 10. Synthesized result of 4-bit Vedic Multiplier

The logic implementation of reversible logic gate is shown in Fig 7 and 8. The simulation output of reversible logic gate is shown in Fig 7. The synthesized RTL model of reversible logic gate is shown in Fig 8. The logic implementation of Vedic multiplier with reversible logic gate is shown in Fig 9 and 10. The simulation output of Vedic multiplier is shown in Fig 9. The synthesized RTL model of Vedic multiplier is shown in Fig 10. The low power and area efficient logic blocks are integrated to implement ALU. The proposed logic blocks are implemented using Verilog HDL programming language, simulated and synthesized using Xilinx ISE 9.2i software.

4 CONCLUSION

In this paper, the low power and high performance ALU circuit is implemented. The low power and area efficient logic blocks reversible logic based adder and Vedic multipliers are

integrated to construct architecture of ALU resulted that the power dissipation of proposed ALU unit is reduced when compared with the conventional unit. The use of less number of adders in the Vedic multiplier reduce the area and power dissipation of ALU system. The proposed logic blocks are implemented using Verilog HDL programming language, simulated and synthesized using Xilinx ISE 9.2i software. The synthesized output resulted that the proposed technique consumes the 35% of power, area of 23% less and the 17% of high-performance compared to conventional ALU circuit.

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